Amendments to the Claims:

This listing of claims will replace all prior listings of claims in the application.

Listing Of Claims:

Claim 1 (currently amended). An area array semiconductor device comprising:

a circuit wiring substrate having a circuit wiring;

a semiconductor chip having a top face and a bottom face, the bottom face being mounted on the circuit wiring substrate and electrically connected with the circuit wiring; and

a sealing layer composed of a sealing resin positioned on the top face of the semiconductor chip;

wherein the sealing layer is formed such that the sealing layer has an angle of 30 to 60° with respect to a side of the circuit wiring substrate.

Claim 2 (original). An area array semiconductor device according to claim 1, wherein the semiconductor chip is mounted on the circuit wiring substrate such that the semiconductor chip has substantially the same angle as an angle which the side of the sealing layer composed of the sealing resin has with respect to the side of the circuit wiring substrate.

Claim 3 (original). An electronic circuit board comprising:

a printed wiring board as a mother board; and

an area array semiconductor device according to claim 1,

wherein the area array semiconductor device is soldered to the printed wiring board as the mother board.

Claim 4 (original). An electronic circuit board according to claim 3, wherein the area array semiconductor device is soldered to the printed wiring board with a lead-free solder.

Claim 5 (new). An area array semiconductor device comprising:

an insulating interposer having a circuit;

an integrated circuit chip mounted on a top surface of the insulating interposer and electrically connected to the circuit of the interposer, the chip having a plurality of sides, each of the sides being at an angle of 30° to 60° with respect to a corresponding side of the interposer;

a resin encapsulating the chip and a portion of the top surface of the insulating interposer, the resin having a plurality of sides angled at the same angle with respect to the interposer as the integrated circuit chip.

Claim 6 (new). An area array semiconductor device according to claim 5, wherein the angle between the sides of the integrated circuit chip and the interposer is 45°.

Claim 7 (new). An area array semiconductor device according to claim 5, wherein a periphery of the resin does not extend to a peripheral of the interposer.

Claim 8 (new). An electronic circuit board comprising:

a printed wiring board;

an insulating interposer defining an upper and a lower surface, the interposer having a plurality of connecting lands and a plurality of solder balls providing electrical connection to the wiring board; the interposer also having a circuit;

an integrated circuit chip in contact with the interposer and electrically connected to the circuit of the interposer, the chip having a plurality of sides, each of the sides being at an angle of 30° to 60° with respect to a corresponding side of the interposer;

a protective material adapted, in conjunction with the insulating interposer, to provide protection from contamination and moisture in the atmosphere, and the material having a plurality of sides angled at the same angle with respect to the interposer as the integrated circuit chip.

Claim 9 (new). An electronic circuit board according to claim 8, wherein the solder balls are made from a lead-free solder having a melting point greater than 183°C.

Claim 10 (new). An electronic circuit board according to claim 9, wherein the solder balls have a melting point of 220°C.

Claim 11 (new). An electronic circuit board according to claim 8, wherein the material also provides thermal insulation for the chip.

Claim 12 (new). An electronic circuit board according to claim 8, wherein the material is applied to the upper surface of the interposer and entirely encapsulates the chip between the material and the interposer.

Claim 13 (new). An electronic circuit board according to claim 8, wherein the material is a moldable material.

Claim 14 (new). An area array semiconductor device according to claim 1, wherein the semiconductor chip is mounted on the circuit wiring substrate such that a side of the semiconductor chip is arranged parallel to the side of the circuit wiring substrate.